AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of reading data from a memory array comprising:

transferring a plurality of data bits from a memory ~~module~~ array onto [[an]] respective input/output signal [[line]] lines; and

sensing [[the]] at least one of said data bits on a first input/output signal line at a first timing and sensing another of said data bits on a second input/output signal line at a second timing different from said first timing,

wherein said sensing timing is related to ~~based on~~ a capacitance ~~of said~~ associated with said first and second input/output signal [[line]] lines.

2. (Currently Amended) The method of claim 1, wherein said first and second timings comprise a first and second respective delay of sensing said data bits ~~further comprising delaying the sensing of the data based on the capacitance of said input/output signal line~~.

3. (Original) The method of claim 2, wherein a delay for an input/output signal line with a capacitance greater than a threshold is greater than a delay for an input/output signal line with a capacitance less than the threshold.

4. (Withdrawn) The method of claim 3, wherein multiple sensing of said less capacitive input/output signal lines is increased.

5. (Currently Amended) The method of claim 1 further comprising the act of shutting off a control signal controlling a sense amplifier that receives a signal from a low capacitance input/output signal line in a time less than a time for shutting off a control signal controlling a sense amplifier that receives a signal from a high capacitance input/output signal line.

6. (Currently Amended) A column output delay circuit for a memory device comprising:

a first delay device, said first delay device delaying a column enable signal for a first period of time based on a capacitance of a first input/output signal line; and

a second delay device, said second delay device delaying a column enable signal for a second period of time based on a capacitance of a second input/output signal line.

7. (Currently Amended) The circuit of claim 6, wherein said first delay device delays a sensing operation on [[an]] said first input/output signal line having less capacitance, and an accumulation of said first and second delay ~~device~~ devices delays a sensing operation on [[an]] a second input/output signal line having greater capacitance.

8. (Currently Amended) The circuit of claim 6 further comprising:

a first column enable signal produced by said first delay device, and

a second column enable signal produced by a ~~combination~~ serial connection of said first and second delay device.

9. (Currently Amended) A memory device comprising:

a memory array;

a datapath coupled to said memory array by input/output signal lines; and

a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of ~~a particular~~ at least two input/output signal [[line]] lines, when the ~~particular~~ at least two input/output signal ~~line is~~ lines are sensed by said sense amplifiers.

10. (Original) The device of claim 9 further comprising:

output data pads for transmitting data from said memory array; and

combinatorial logic for determining which sense amplifier sends data to said output pads.

11. (Currently Amended) The device of claim 9, wherein said column output delay circuit comprises:

a first delay device that delays a sensing operation on [[an]] a first input/output signal line of a first capacitance, and

a second delay device wherein an accumulation of delays of said first and second delay device delays a sensing operation on [[an]] a second input/output signal line having a second capacitance greater than said first capacitance.

12. (Currently Amended) The device of claim 11, wherein said column output delay circuit further comprises:

a first column enable signal produced by said first delay device, and

a second column enable signal produced by a ~~combination~~ serial connection of said first and second delay device.

13. (Original) The device of claim 12, wherein said first and second column enable signals control said sense amplifiers.

14. (Original) A processor system comprising:

a processor; and

a memory device, said memory device comprising:

a memory array,

a datapath coupled to said memory array by input/output signal lines, and

a column output delay circuit, said circuit coupled to sense amplifiers in said datapath for controlling, based on a capacitance of ~~a particular~~ at least two input/output signal [[line]] lines, when the ~~particular~~ at least two input/output signal ~~line is~~ lines are sensed by said sense amplifiers.

15. (Currently Amended) The system of claim 14, wherein said column output delay circuit comprises:

a first delay device that delays a sensing operation on [[an]] a first input/output signal line of a first capacitance, and

a second delay device wherein an accumulation of delays of said first and second delay device delays a sensing operation on [[an]] a second input/output signal line having a second capacitance greater than said first capacitance.

16. (Currently Amended) The system of claim 15, wherein said column output delay circuit further comprises:

a first column enable signal produced by said first delay device, and

a second column enable signal produced by a ~~combination~~ serial connection of said first and second delay device.

17. (Original) The system of claim 16, wherein said first and second column enable signals control said sense amplifiers.